LISTING OF THE CLAIMS

1. - 8. Canceled

9. (Currently Amended) A power MOSFET having reduced on resistance comprising:

a ~~P type~~ P+ conductivity substrate; an epitaxially deposited ~~N type~~ N+ conductivity layer deposited atop said ~~P type~~ P+ substrate to form an epitaxial layer having a substantially uniform concentration of N type dopants throughout its volume; a plurality of spaced stripe trenches having vertical walls extending through said epitaxial layer into said P+ conductivity substrate; a thin gate oxide on said vertical walls and conductive polysilicon with a P type conductivity deposited into said trenches to define a polysilicon gate; ~~a P type~~ P+ concentration source region stripes formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a plurality of spaced notches extending through said source regions and exposing said epitaxially deposited layer; an N++region formed in said N+ epitaxially deposited layer at bottom of each notch; a source contact connected to at least said source regions; and a drain contact made of metal and connected to a bottom surface of said substrate, wherein the doping of said ~~N-type~~ N++ epitaxially deposited layer allows reverse voltage to be blocked therein and wherein said source contact extends through said plurality of notches and is connected to each said N++ region.

10. Canceled

11. (Currently Amended) The MOSFET of claim [[10]] 9, wherein said epitaxial layer has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

12. (Previously Presented) The MOSFET of claim 9, wherein said substrate is a P^+ substrate having a resistivity of less than about 0.005 ohm cm.

13. Canceled

14. - 22. (Canceled).

23. (New) The MOSFET of claim 9, wherein said substrate is not thicker than 210 μm.